

AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions and listings of claims in the application:

Listing of Claims

A2 1. (original) A method of selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and at least one memory module comprising a serial presence detect memory, said method comprising:

counting the number of said memory modules;
generating multiple clock frequencies to
provide selectable operating speeds of said memory module interface; and

selecting one of said operating speeds of said memory module interface in accordance with said counting.

2. (original) The method of claim 1 wherein said selecting comprises generating memory module interface signals comprising clock, address, and data signals at a frequency based on said memory module count.

3. (original) The method of claim 1 further comprising obtaining information from said serial presence detect memory that includes at least one characteristic of said memory module, wherein said selecting comprises selecting one of said operating speeds in accordance with one of said counting and said characteristic.

4. (original) The method of claim 3 wherein said characteristic comprises the number of components in each said memory module.

5. (original) The method of claim 3 wherein said characteristic comprises a speed grade of said memory module.

6. (original) The method of claim 3 wherein said characteristic comprises a manufacturer of said memory module.

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7. (original) The method of claim 3 wherein said characteristic comprises a type of said memory module.

8. (original) The method of claim 3 wherein said characteristic comprises a physical layout of signal connections between said memory controller and said memory module.

9. (currently amended) A method of selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and at least one memory module comprising a serial presence detect memory, said method comprising:

generating multiple clock frequencies to provide selectable operating speeds of said memory module interface;

counting the number of said memory modules;
obtaining information from said serial presence detect memory that includes at least one characteristic of said memory module; and

selecting said operating speed of said memory module interface in accordance with at least one of said counting and said obtaining information.

10. (original) The method of claim 9 wherein said characteristic comprises a type of said memory module.

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11. (currently amended) A method of selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and at least one memory module comprising a serial presence detect memory, said method comprising:

~~counting the number of said memory modules;~~
generating multiple clock frequencies to
provide selectable operating speeds of said memory module
interface;

obtaining information from said serial presence detect memory that includes at least the number of components in each said memory module; and

selecting said operating speed of said memory module interface in accordance with ~~at least one of said~~
~~counting and~~ said obtaining information.

12. (currently amended) A method of selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and at least one memory module comprising a serial presence detect memory, said method comprising:

~~counting the number of said memory modules;~~
generating multiple clock frequencies to
provide selectable operating speeds of said memory module
interface;

obtaining information from said serial presence detect memory that includes at least a speed grade of said memory module; and

selecting said operating speed of said memory module interface in accordance with ~~at least one of said~~
~~counting and~~ said obtaining information.

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13. (original) A computer system comprising:
a central processing unit;
a memory controller including a memory module
interface; and
at least one memory module including a serial
presence detect memory; wherein said memory controller:
generates multiple clock frequencies;
accesses said serial presence detect memory;
keeps a running tally of the number of said
memory modules based on said accesses to said serial presence
detect memory; and
selects one of said clock frequencies for
driving said memory module interface based on at least a final
tally of the number of said memory modules.

14. (original) The computer system of claim 13
wherein said central processing unit is a microprocessor.

15. (original) The computer system of claim 13
wherein said memory controller obtains information from said
serial presence detect memory that includes at least one
characteristic of each said memory module.

16. (original) The computer system of claim 15
wherein said characteristic comprises the number of components
in each said memory module.

17. (original) The computer system of claim 15
wherein said characteristic comprises a speed grade of said
memory module.

18. (original) The computer system of claim 15 wherein said characteristic comprises a manufacturer of said memory module.

19. (original) The computer system of claim 15 wherein said characteristic comprises a type of said memory module.

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20. (original) The computer system of claim 15 wherein said characteristic comprises a physical layout of signal connections between said memory controller and said memory module.

21. (currently amended) A computer system comprising:

a central processing unit;

a memory controller including a memory module interface and at least two phase locked loops to generate respective clock signals of different frequencies;

at least one memory module including a serial presence detect memory; wherein said memory controller:

accesses said serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least one characteristic of said memory module; and

provides a memory module interface at a clock rate based on at least one of a final tally of the number of said memory modules and said obtained information.

22. (original) The computer system of claim 21 wherein said characteristic comprises the number of components in each said memory module.

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23. (currently amended) A computer system comprising:

a central processing unit;

a memory controller including a memory module interface and at least two phase locked loops to generate respective clock signals of different frequencies;

at least one memory module including a serial presence detect memory; wherein said memory controller:

accesses said serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least the number of components in each memory module; and

provides a memory module interface at a clock rate based on at least one of a final tally of the number of said memory modules and said obtained information.

24. (currently amended) A computer system comprising:

a central processing unit;

~~a memory controller including a memory module interface~~ and at least two phase locked loops to generate respective clock signals of different frequencies;

at least one memory module including a serial presence detect memory; wherein said memory controller:

accesses said serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least a speed grade of said memory modules or their components; and

A2 provides a memory module interface at a clock rate based on at least one of a final tally of the number of said memory modules and said obtained information.

25. (original) A computer system comprising:

a central processing unit;

at least one memory module including a serial presence detect memory; and

memory controller means including memory module interface means; wherein said memory controller means:

generates multiple clock frequencies;

accesses serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory; and

selects one of said clock frequencies for driving said memory module interface means at a clock rate based on at least a final tally of the number of said memory modules.

~~26. (currently amended) A computer system~~
comprising:

a central processing unit;

at least one memory module including a serial presence detect memory; and

memory controller means including memory module interface means and means for generating multiple clocks at different frequencies; wherein said memory controller means:

accesses serial presence detect memory;
keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least one characteristic of said memory module; and

provides a memory module interface means at a clock rate based on at least one of a final tally of the number of said memory modules and said obtained information.

27. (original) The computer system of claim 26 wherein said characteristic comprises a type of said memory module means.

28. (original) The computer system of claim 26 wherein said characteristic comprises a physical layout of signal connections between said memory controller means and said memory module means.

29. (currently amended) A computer system comprising:

a central processing unit;
~~at least one memory module including a serial~~
presence detect memory; and

memory controller means including memory module interface means and means for generating multiple clocks at different frequencies; wherein said memory controller means:
accesses serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least the number of components in each memory module means; and

provides a memory module interface means at a clock rate based on at least one of a final tally of the number of said memory modules and said obtained information.

30. (currently amended) A computer system comprising:

a central processing unit;

at least one memory module including a serial presence detect memory; and

memory controller means including memory module interface means and means for generating multiple clocks at different frequencies; wherein said memory controller means:

accesses serial presence detect memory;

keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

obtains information from said serial presence detect memory that includes at least a speed grade of said memory module or its components; and

provides a memory module interface means at a ~~clock rate based on at least one of a final tally of the~~ number of said memory modules and said obtained information.

31. (currently amended) A memory controller comprising a memory module interface to at least one memory module, said memory module including serial presence detect memory; wherein said memory controller:

generates multiple clocks at different frequencies

accesses serial presence detect memory;
keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory; and

provides a memory module interface at a clock rate based on at least ~~at least~~ a final tally of the number of said memory modules.

32. (original) The memory controller of claim 31 wherein said memory controller obtains information from said serial presence detect memory that includes at least one characteristic of said memory module wherein said clock rate is also based on said characteristic.

33. (currently amended) The memory controller of claim [[31]] 32 wherein said characteristic comprises the number of components of said memory module.

34. (currently amended) The memory controller of claim [[31]] 32 wherein said characteristic comprises a speed grade of said memory module.

35. (currently amended) The memory controller of claim [[31]] 32 wherein said characteristic comprises a manufacturer of said memory module.

36. (currently amended) The memory controller of claim [[31]] 32 wherein said characteristic comprises a type of said memory module.

37. (currently amended) The memory controller of claim [[31]] 32 wherein said characteristic comprises a physical layout of signal connections between said memory controller and said memory module.

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38. (original) A memory controller comprising a memory module interface to at least one memory module, said memory module including serial presence detect memory; wherein said memory controller:

- generates multiple clock frequencies;
- accesses serial presence detect memory;
- keeps a running tally of the number of said memory modules based on said accesses to said serial presence detect memory;

- obtains information from said serial presence detect memory that includes at least one characteristic of said memory module; and

- selects one of said clock frequencies for driving said memory module interface based on at least one of a final tally of the number of said memory modules and said obtained information.

39. (original) The memory controller of claim 38 wherein said characteristic comprises a speed grade of said memory module.

~~40. (currently amended) A memory controller~~
comprising a memory module interface to at least one memory module and at least two phase locked loops to generate respective clock signals of different frequencies, said memory module including serial presence detect memory; wherein said memory controller:

- accesses serial presence detect memory;

obtains information from said serial presence detect memory that includes at least the number of components in said memory module; and

provides a memory module interface at a clock rate based on said obtained information.

A2 41. (original) A memory controller comprising a memory module interface to at least one memory module, said memory module including serial presence detect memory; wherein said memory controller:

accesses serial presence detect memory;
generates multiple clock frequencies;
obtains information from said serial presence detect memory; and

selects one of said clock frequencies for driving said memory module interface based on said obtained information.

42. (original) The memory controller of claim 41 wherein said obtained information comprises a speed grade of said memory module.

43. (original) Apparatus for selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and at least one memory module comprising a serial presence detect memory, said apparatus comprising:

means for counting the number of said memory modules;

means for generating multiple clock frequencies to provide selectable operating speeds of said memory interface; and

means for selecting one of said multiple clock frequencies to provide an operating speed in accordance with said counted memory modules.

A2 44. (original) The apparatus of claim 43 wherein said selecting comprises means for generating memory module interface signals comprising clock, address, and data signals at a frequency based on said memory module count.

45. (original) The apparatus of claim 43 further comprising means for obtaining information from said serial presence detect memory, said information including at least one characteristic of said memory module; wherein said means for selecting selects one of said multiple clock frequencies in accordance with at least one of said number of counted memory modules and said obtained information

46. (currently amended) The apparatus of claim [[43]] 45 wherein said characteristic comprises the number of components in each said memory module.

47. (currently amended) The apparatus of claim [[43]] 45 wherein said characteristic comprises a speed grade of said memory module.

48. (currently amended) The apparatus of claim [[43]] 45 wherein said characteristic comprises a manufacturer of said memory module.

49. (currently amended) The apparatus of claim [[43]] 45 wherein said characteristic comprises a type of said memory module.

50. (currently amended) The apparatus of claim [[43]] 45 wherein said characteristic comprises a physical layout of signal connections between said memory controller and said memory module.

51. (currently amended) Apparatus for selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and at least one memory module comprising a serial presence detect memory, said apparatus comprising:

means for counting the number of said memory modules;

means for generating multiple clocks at different frequencies;

means for obtaining information from said serial presence detect memory that includes at least one characteristic of said memory module; and

means for selecting said operating speed of said memory module interface in accordance with at least one of said means for counting and obtaining information.

52. (currently amended) Apparatus for selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, a memory controller, and at least one memory module comprising a serial presence detect memory, said apparatus comprising:

~~means for counting the number of said memory~~
modules;

means for generating multiple clocks at different frequencies

means for obtaining information from said serial presence detect memory that includes at least the number of components in each said memory module; and

means for selecting said operating speed of said memory module interface in accordance with at least one of said means for counting and obtaining information.

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53. (currently amended) Apparatus for selecting an operating speed of a memory module interface in a computer system, said system comprising a central processing unit, and a memory controller, and at least one memory module comprising a serial presence detect memory, said apparatus comprising:

means for counting the number of said memory modules;

means for generating multiple clocks at different frequencies

means for obtaining information from said serial presence detect memory that includes at least a speed grade of said memory module; and

means for selecting said operating speed of said memory module interface in accordance with at least one of said means for counting and obtaining information.
